Fermilab

HRM-II Remote Unit

Revised 5 September 2006

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I. Introduction

The HRM-II remote unit is a completely redesigned follow-on to the HRM remote unit presented at the 2001 ICALEPCS. It features:

- an ADSP-2191 DSP as the main processor with an instruction clock rate of 160Mhz
- A high-speed serial link using the Cypress Hot-Link chip set
- a DMA controller optimized for HRM-style data transfer
- the ability for the DMAC and the DSP to concurrently access plug-in I/O modules
- an on-board TCLK receiver modeled after the IP-177 module
- a single port interface for snapshot, slow MADC, medium-speed MADC, and digital I/O modules
- the ability to mix-and-match I/O modules in a single chassis subject to restrictions

The DSP sets up the system and coordinates data transfers between the I/O modules (IOMs) and the Hot-Link; it is not directly involved in the transfers. The DSP has its own dedicated FIFO port for DMA and can access any of the IOMs. Thus, the DSP is available to pre-process IOM data and forward it on to the serial link.

II. Overview (refer to block diagram and schematic)

Board Support

A 40Mhz oscillator supplies a free-running clock to all IOM sockets, to the FPGAs, and to the DSP.

The FPGA 3.3V supply is regulated from the 5V VCC plane by a LT1085 low-dropout linear regulator (U40). This also provides the I/O supply for the DSP.

The core of the DSP runs off of 2.5V provided by a LT1117 low-dropout regulator (U41).

Positive and negative 24V enters the board at connector J16 and is routed to the IOM sockets. Each supply is fused. The central board does not use either of the analog voltages. A separate analog return is routed to the port connectors. A jumper allows the analog return and the logic return to be connected at a single point near J16. The case fan

is driven from the negative 24V via header J1. The case fan is also the minimum load that keeps the -24V supply in regulation.

DSP

The DSP is an Analog Devices 16 bit fixed point processor. It was selected for its high speed and its need for a minimum of external support. The external memory port of the DSP is used as a general system bus. No use is made of the host port or the synchronous serial ports.

System reset is driven by a DS1832 watchdog (U4). The 1832 makes a reset if the 3.3V supply drops below 3V, in response to a front-panel pushbutton, and if its strobe is not toggled within a 1 second timeout delay. A free-running timer (U5) may be jumpered to the strobe to defeat the watchdog function during firmware development.

The DSP can be configured to boot either from EEPROM (U11) or via the RS232 diagnostic port (U3) by setting jumper JU3. The internal UART boot program does not seem to work according to the published rules and Analog has been unresponsive to repeated inquiries. If the ability to download code from a PC is needed, you should use an EEPROM that is burned with MON2191. This handy monitor program will not only download code through the UART, but it also has a number of other handy commands that a developer will find useful.

Rev B and Rev C boards have the EEPROM on a kludge board that gates 5V to the part only after the 5V has ramped above 4.7v. Xicor/Intersil parts seem to dislike a slow power ramp while Catalyst parts work fine. Intersil was unresponsive in addressing this problem. The VCC switch will be added to subsequent revisions of the central board.

The DSP comes up from reset in BYPASS mode with its internal clock multiplier PLL disabled and the core driven directly from the 40Mhz system clock. As part of the initialization process the clock control registers of the DSP should be re-configured for 160Mhz core clock and 80Mhz HCLK to extract all available MIPS from the device. A pair of Dallas DS1250 SRAM modules (U12, U13) provides 128K x 16 of non-volatile data memory beyond the 32K of internal DM, albeit at the slower external bus access speed. Because the 2191's inputs are not 5V-tolerant, a bi-directional buffer (U9, U10) is placed in series with the 5V-only devices that drive the system bus.

Header P2 is provides a connection to an Analog emulator pod. Analog literature suggests that jumpers be placed across 5-6, 7-8, 9-10, and 12-11 when the emulator is absent.

TCLK

A 10K30 Altera FPGA (U21) decodes TeV Clock and drives eight rear-panel outputs. All TCLK-related I/O is on 34-pin header J15. 74F3037 line drivers drive all TCLK outputs.

TCLK is received and discriminated by a MAX902 comparator (U22B). A carrier detect comes from U22A. Received TCLK is also routed to each IOM connector for local use.

The TCLK logic is modeled after the IP-177. The register map is similar to that of the IP-177 and all register fields and functions are identical. Each of the eight outputs has a separate event map and is programmable in delay and width. Even and odd outputs can be cascaded ("daisy-chain mode"). For details on operation, refer to the "IP-177 Eight Channel Delay Timer" design note by McClure, et.al., 22 January, 1998.

Three additional programmable event decoders are dedicated to internal functions. The Trigger Event decoder generates a timing pulse on the trigger input of each IOM port. The DMA Event decoder generates a timing pulse that can be used to initiate a DMA sequence. The Synchronization Decoder generates a pulse that interrupts the DSP to allow the free-running timestamp counters to be correlated to an event and to each other. Each of these decoders outputs a 100nsec-wide pulse in response to a single software-programmable event. There are no delay counters associated with them.

Timestamp correlation is handled with a combination of hardware and software. The correlation event decoder captures the value of a 32-bit free-running counter on the central board and posts an interrupt to the DSP. The DSP TCLK interrupt service reads and saves the value and sets a flag. When the flag is set, the DMA interrupt service captures the present value of the central board FRC and of the timestamp counters on all modules. The offset between the current FRC and the saved FRC is subtracted from each timestamp value to yield the value of the timestamp when the correlation event occurred. These values are then written to the PMC over the hot-link.

HOT-LINK

The Hot-Link section is the means used to link the HRM remote unit to a Controls Front-End. There are two physical interfaces for the serial link. A PCB stuff option accepts a standard 1x9 optical module for a fiber optic medium. The copper interface is transformer coupled. The Hot-Link front panel connector is a Fiber Channel standard HSSDC-I connector. Pre-assembled cables using the mating connectors are available from Methode, AMP, Molex, and others. Connectors are available from Circuit Assembly. The Hot-Link normally operates at 320 Mbps. To span longer distances, a 160 Mbps low-speed mode can be selected by jumpering two pins in the HSSDC cable plug. The Hot-Link circuitry used here is identical to that used on the HRM PMC.

Receiver

The incoming serial stream is de-serialized by Hot-Link receiver chip U33. Received bytes are loaded into the 8K x 9 receiver FIFO (U31). The packet disassembler resides inside the RXCHIP FPGA (U2). The disassembler searches the FIFO for a packet framing byte and reads the next four bytes to form an address word and a data word. When a complete packet has been read out, an interrupt is signaled and the disassembler waits for DSP software to read it. Data arriving from the front-end consists of occasional

control register settings and digital output register updates and thus there is no need for specialized hardware to handle it.

The RXCHIP also supports the built-in test functions of the Hot-Link chipset. A pair of twelve-bit counters keeps track of the number of test loops received and the number of receiver errors. Link status is also read out through this device.

RXCHIP has a software readable 32-bit free-running counter available for timestamping and general use. The counter is clocked at 1Mhz.

Transmitter

The DMA Controller, to be discussed in the next section, feeds the Hot-Link transmitter. The DMAC routes the outbound byte stream into the 8K x 9 transmit FIFO (U32). The FIFO is read and serialized by Hot-Link transmitter U34.

Hot-Link Control

The serial link is controlled by logic in the EPM7032 Hot-Link Control FPGA (U30). A clock divider divides a 64 Mhz input by either two or four to make a transmitter write clock. Logic monitors the outputs of the receiver chip and flags receiver overrun, 8B/10B code errors, and out-of-sequence link-control codes. The FPGA negotiates the handshaking between the transmit and receive FIFOs and their corresponding Hot-Link device.

DMA

The HRM-II uses a unique DMA scheme to speed data from the I/O modules to the Hot-Link while giving the DSP simultaneous access to them. All DMA accesses are read operations.

DMA Control Registers

There seven registers are used by the DSP to control operation of the DMAC:

- Port A through Port D count registers
    - The count registers are ten-bit registers that determine the maximum number of transfers that a port will do in any single DMA cycle. These registers are write-only.
- Skip Register
    - A bit set in the Skip Register tells the DMAC to bypass the corresponding port. The Skip Register is R/W.
- End-of-data Control Register
    - A bit set in the EODC register tells the DMAC to not set the skip flag when the port signals end-of-data. This means that the DMA will recur on the next cycle. Clearing the EODC bit tells the DMAC that the IOM did a one-shot acquisition. On EOD, the DMAC will set the skip flag and ignore

the port on subsequent cycles. For example, a snapshot card will empty its FIFO over a number of DMA cycles and signal EOD when its FIFO is empty. With EODC=0, the DMAC sets the skip bit and no further DMA action will occur to the snapshot port until the DSP sets up the next snapshot. For a 64 channel slow MADC, EOD will be signaled every DMA cycle. Because EODC=1, skip remains off and the DMAC will check the MADC card every cycle. The EODC Register is R/W.

- DMA Status Register

  The Status register has four bits that indicate which of the four ports is currently running a DMA. Reading the status port will block the start of the next DMA long enough for the DSP to test the busy flag and then access an inactive port.

- Reset register

  Writing to the reset register does a hardware reset on the DMAC

DMA Time Structure

A DMA cycle is initiated by a 80 ns-wide tick from a hardware timer on the ADSP-2191 that repeats every 100 usec. (FRMTICK) (For correct operation of the DMAC, DSP software needs to set the TIMER0 pulse width as specified.) Upon receipt of the frame tick, the DMAC broadcasts a /DMABGN pulse to all of the DMA ports. This signal is intended to initialize the IOMs for the coming DMA.

The DMAC next checks the SKIP flag of Port A. If set, the DMAC proceeds to Port B. If clear, the DMAC asserts /DMAC. /DMAC tells the IOM that the current port cycle is originating from the DMAC. The IOM drives the address bus with type code and channel number and drives the data bus with a data word. It also drives /EOD and /DAV. Read strobe is asserted by the DMAC if it sees that data is available. /RD stays asserted until the IOM asserts /RDY. On recognizing /RDY, the DMAC rescinds /RD and /DMAC, latches the address and data words, and passes them onto the Hot-Link transmitter. After a brief idle time, the process repeats. On termination of Port A's DMA, the DMAC proceeds to Ports B, C, and D in sequence. When finished with Port D, the DMAC idles until the next FRMTICK. If a tick occurs while the DMAC is busy, the DMAC resets and begins a new frame.

Burst DMA Mode (sw v1.08+)

When the "DMA Frame TCLK Trigger Enable" register (48 0082) is non-zero, DMA is initiated by the "TCLK DMA Event" decoder (48 00DE). The decoder resets a 100us timebase and starts a DMA frame counter. Successive DMAs occur every 100us until the frame count expires. The decoder is re-armed after the count expires.

DMA Termination Conditions

Several conditions will cause the DMAC to stop reading a port until the next frame. Normal termination occurs when the port word counter becomes zero. The maximum

number of words for the current cycle has been read and it's the next port's turn. DMA will also end if /DAV is not asserted with /EOD inactive. This means that the IOM is still acquiring data but its buffer has been emptied. The DMAC will check again during the next frame. All DMA activity will pause if the Hot-Link transmit FIFO becomes full. DMA will also stop if EOD becomes active with DAV inactive, signaling that IOM's buffer is empty and nothing further is expected. Note that there is no timeout on /RDY; an IOM that withholds /RDY will hang the DMAC until the next frame.

DualPort Access Feature

A two-by-four bidirectional switch arrangement allows the DSP to access the IOM ports at the same time that the DMAC is running. Each port has a private address and data bus connected to a corresponding switch. The switch will connect X (DSP) and Y (DMAC) to any A, B, C, or D without restriction. Unlike a conventional single bus design, the DSP does not need to wait for the DMAC to finish the entire DMA before it can use the ports. Unlike a conventional dual-ported design, IO modules do not need to support two completely independent buses. The only restriction imposed on the two masters is that they do not access the same port at the same time.

Software can use the channel BSY flags in the status register to determine where the DMAC is currently reading. (A cycle-by-cycle arbitration scheme could have been used, but would have slowed all accesses by requiring additional time to regenerate read and write strobes.) Reading the status blocks the DMAC from advancing to the next channel long enough for the DSP to complete a subsequent read or write to an IOM. Port D is not subject to any access restrictions.

Port D

Port D is a 32-bit wide, 4K deep FIFO buffer attached to the DSP. The DSP writes sets of data and address words to Port D for readout by the DMAC. Normally, Port D will be used by the DSP to send periodic updates of various "virtual" set-up and status registers to the HRM PMC. Port D can also be used to create "virtual" IOMs. Port D /DAV is tied to the FIFO EMPTY flag inverted and /EOD to EMPTY flag so that FIFO empty ends the transfer.

Remote Unit to PCI Interrupt

An interrupt can be posted to the PCI interface at the host by sending a packet with typecode = 0xB from the remote unit to the PMC. The data and address fields are discarded at the PMC. The special typecode packet can either be loaded by DSP software into Port D or incorporated into the stream from an IOM.

Required IOM Features

Because of the unique DMA capability, IO modules must have some capabilities beyond those associated with typical slave-only devices.

First, the DMAC is deliberately kept ignorant of parameters specific to the IOMs. Its function is to transport data from the IOMs to the Hot-Link. Each IOM must provide data to the Hot-Link in the correct format and in the correct sequence. This means that the IOM must be able to insert its own timestamps, typecodes, channel numbers/register addresses, and data into the output stream. The DMAC depends on the IOM to close a transfer via /EOD and /DAV; the total length of a transfer is completely under the control of the IOM.

The address bus into each port is bi-directional. The port drives address into the IOM for DSP accesses (/DMAC=1) and the IOM drives addressing data into the port for DMA accesses.

The DSP reads the /RDY input of each board to determine if an IOM is present. Therefore, an IOM must drive its /RDY to VCC when it is not being accessed for board detection to work.

To assist the DSP in configuring the system, an IOM needs to provide a single 16 bit read/write register at address $0000. A read of the ID register gives the DSP an IOM model number and a version number. A DSP write of the ID register sets up the typecodes the IOM will attach to its timestamps and data. Using loadable typecodes means that more than one of a module type can be used in a single remote chassis.

MADC and snapshot boards must insert a 32-bit timestamp at the appropriate location in their data stream. This timestamp may be derived from a free-running counter. A 1Mhz clock is available at the port connector for this purpose. The clock is a divide from the 10MHz TCLK carrier. If TCLK is lost, the DSP may switch the clock source to either an external signal or the on-board 40Mhz oscillator. ***The DSP must be able to capture and read a timestamp from any MADC board to allow the counter to be correlated with TCLK events.*** This requirement is optional for snapshot boards since snapshot data is acquired in response to an event trigger. A DSP read of one of the 16-bit timestamp registers must also latch the other timestamp register.

An I/O module needs to be aware of how the data stream it generates will be handled on the PMC-end of the link. This means that the module needs to insert timestamps at the correct place and that data is sent in the correct sequence to be placed into memory on the PMC.

Port Utility Signals

Port connectors are supplied with a set of utility signals:

- /RESET – system reset
- 1 Mhz – timestamp counter clock
- CLK - 40 Mhz utility clock
- /ARM – separate line for each port; software-generated arming signal
- /TRIG – separate line for each port; IP177 event trigger

- TCLK – raw TCLK from the TCLK receiver (U22B)

DMA Circuitry

DMA circuitry is scattered about the central board. FPGA U19 is the address switch and FPGA U20 is the data switch. The DMAC is contained within FPGA U18. The chip select decoding for U18 resides in FPGA U2 (RXCHIP). Port D is FIFOs U14 through U17.

III. Jumpers

Watchdog

	JU1	JU2
Normal Operation	ON	OFF
Development and Testing	OFF	ON

Boot

	JU3
UART boot	OFF
EEPROM boot	ON

Analog Return

	JU4
No connection to DGND	OFF
Connected to DGND	ON

IV. I/O Module Connector Signal Names and Definitions

D0-D15	Bidirectional	16	Data
/RD	Input	1	Read timing strobe. Data valid at L>H.
/WR	Input	1	Write timing strobe. Data valid after H>L and held past L>H.
/DMAC	Input	1	Driven low to indicate DMAC read access
/TRIG	Input	1	Starts an acquisition cycle, resets the FIFOs, and clears End-of-Data. From central brd trigger logic.
/ARM	Input	1	Stops acquisition in progress, resets slave logic, asserts End-of-Data, and readies slave for trigger. FIFOs are not reset (readout continues). From central brd trigger logic.
/DAV	Std-Output	1	Indicates to the DMAC there data is available for readout in the buffer.
/DMABGN	Input	1	H>L indicates start of new 100us DMA period
/EOD	Std-Output	1	Indicates to DMAC that the slave has taken

			the requested number of samples and is now inactive. (End-of-data can be asserted before buffer readout is finished. The DMAC stops on end-of-data and no-data-available.)
A0-A15	Bidirectional		To slave from DSP, from slave for DMAC
- TC/DSP Adrs		4	DMAC TC0-3, DSP A12-A15
- Cnl Nr/DSP Adrs		12	DMAC CNL0-11, DSP A0-A11
/RDY	Std-Output	1	Slave response to Read and Write. Always driven by slave.
/RESET	Input	1	System reset
CLK	Input	1	Free-running 40 MHz clock
1MHZ	Input	1	Free-running 1 MHz clock
VCC	To Slave	6	5V logic power
DGND	From Slave	12	Logic return*
VDD	To Slave	2	24V analog power
VEE	From Slave	2	Negative 24V analog power
AGND	From Slave	4	+24V and –24V analog return*
TCLK	To Slave	1	Buffered 10 Mhz TCLK input gated with carrier detect
(Spare)		9	

*I/O connector shells and module front panels return to chassis (safety) ground through mechanical connections and not through supply returns

1. All reads and writes are 16 bits. There are no 8 bit operations.
2. Std-Output: Always-on output.
3. Bidirectional: Input or output depending on DMAC, /RD, /WR, and /ID. Tristated otherwise.
4. All port signals are 3.3v except the 1Mhz and TCLK, which are 5v. All port signals are 5v tolerant.

V. HRM I/O Module Pinout

Connector: AMP MODU System 50 80 pin 1-104118-6 (mates to 103911-6 on central board)

Pin		Pin	
1	DGND	2	CLK
3	/RESET	4	DGND
5	D1	6	D0
7	D3	8	D2
9	D5	10	D4
11	D7	12	D6
13	DGND	14	VCC
15	D9	16	D8
17	D11	18	D10

19	D13	20	D12
21	D15	22	D14
23	DGND	24	VCC
25	A1	26	A0
27	A3	28	A2
29	A5	30	A4
31	A7	32	A6
33	DGND	34	VCC
35	A9	36	A8
37	A11	38	A10
39	A13	40	A12
41	A15	42	A14
43	DGND	44	VCC
45	/WR	46	/RD
47	/RDY	48	DMAC
49	/DAV	50	/EOD
51	DGND	52	VCC
53	/TRIG	54	/ARM
55	DGND	56	VCC
57	DGND	58	DGND
59	/DMABGN	60	1MHZ
61	Spare	62	TCLK
63	Spare	64	Spare
65	DGND	66	DGND
67	Spare	68	Spare
69	Spare	70	Spare
71	Spare	72	Spare
73	AGND	74	VEE
75	AGND	76	VEE
77	AGND	78	VDD
79	AGND	80	VDD

VI. Required I/O Module Registers

Timestamp

Snapshot ADC and Multiplexed ADC cards must provide a 32-bit timestamp with 1 usec resolution. The timestamp is read out in two 16-bit segments, most-significant word followed by least-significant word. For Mux-ADC cards, the timestamp must be read out at the start of every DMA cycle and before any of the channel data is transferred. For Snapshot-ADC cards, the timestamp is read before any snapshot data is transferred, but only once per snapshot. A type-code and an MSW/LSW flag accompany each word of timestamp data on the address lines.

15 12	11 ADRS 1	0
Timestamp Typecode	0000 0000 000	MSW Flag=1

15 DATA 0
MS Timestamp

15 12	11 ADRS 1	0
Timestamp Typecode	0000 0000 000	MSW Flag=0

15 DATA 0
LS Timestamp

ID Register

All cards will have a sixteen-bit read-only ID register. The ID register resides at address $0. The central board uses the value returned from the ID register to configure software support for the card.

DSP Adrs=$0000 & RD

15 8	7 0
Card Model ID	Card Version

Model ID assignments are:

10Khz MADC (“Slow MADC”)	0x72
100Khz MADC (“Fast MADC”)	0xB8
Snapshot	0x1D
Digital IO	0x4E

Typecodes Register

Cards provide an 8-bit write-only typecodes register. This feature enables support of multiple cards of one type in an HRM chassis.

DSP Adrs = $0000 & WR

15 8	7 4	3 0
0000 0000	Timestamp Typecode	Data Typecode

VII. I/O Module Mechanical Specification

Overall board dimensions: 7.000 in wide by 5.825 deep

Standard connector placements: see drawing (IOMs may use any connectors in any combination, though doing so will require changing the rear panel cut-outs)

Mounting hole diameters and locations: see drawing

Plug-in module plug: AMP MODU System 50 right angle plug, 80 pin, 1-104118-6

I/O module attachment: Richco SRS4-3-01 3/16” self-retaining spacers space central board and modules above the chassis floor. Either 4-40 machine screws (requires threaded PEM inserts in the chassis) or #4 self-tapping screws may be passed through the spacers to secure the boards

VIII. I/O Module Timing Specification

All timing specifications are subject to change without notice and may even be plain wrong at this time

DSP Read Cycle
Address valid to /RD active: 15 ns min
Data valid to /RD inactive: 15 ns min
Hold, /RD inactive to address: 0 ns min
Hold, data valid past /RD inactive: 0 ns min
/RD recovery (/RD high between cycles): 25 ns min
Hold, /RDY past /RD inactive: 0 ns min

DSP Write Cycle
Setup, address to /WR active: 15 ns min
Data valid to /WR active: 15 ns min
Hold, /WR inactive to address: 0 ns min
Hold, data valid past /WR inactive: 0 ns min
/WR recovery (/WR high between cycles): 25 ns min
Hold, /RDY past /WR inactive: 0 ns min
Setup, /RDY to /WR inactive: TBD

DMAC Read Cycle
Setup, DMAC to /RD active: 10 ns min
Address valid to /RD active: 15 ns min
Data valid to /RD inactive: 15 ns min
Hold, /RD inactive to address: 0 ns min
Hold, data valid past /RD inactive: 0 ns min
/RD recovery (/RD high between cycles): 25 ns min
Hold, /RDY past /RD inactive: 0 ns min
Setup, /RDY to /RD inactive: TBD

IX. Central Board DSP I/O Port Addresses and Bit Definitions

Off-Chip DSP Memory Map

	2191 Select	Page	Address Range
DMAC	IOMS	IO $08	$0200-$021F
RXCHIP	IOMS	IO $08	$0240-$025F
TCLK	MS0	DM $01	$0000-$01FF

External SRAM	MS0	DM $02-$03	$0000-$FFFF
Port D Data FIFO	MS1	DM $40	$0000-$FFFF*
Port D Adrs FIFO	MS2	DM $80	$0000-$FFFF*
Port A	MS3	DM $C0	$0000-$FFFF
Port B	MS3	DM $C1	$0000-$FFFF
Port C	MS3	DM $C2	$0000-$FFFF
EEPROM**	BMS	BM	$0000-$FFFF

*No addresses are uniquely decoded. Firmware may use a buffer copy to load the FIFO.
**Byte addressing

Programmable Flag Pins

	Direction	Function
PF0	Input	TCLK Event Decoder IRQ input
PF1	Input	RX IRQ input
PF2	Input	DMA Done IRQ input
PF3	Input	X
PF4	Output	Heartbeat LED
PF5	Output	Link loopback test
PF6	Output	Link reset
PF7	Output	Watchdog kick

DMAC I/O

IO & $08:200 & W – Port A Count

15 10	9 0
x	Transfer Count

IO & $08:201 & W – Port B Count

15 10	9 0
x	Transfer Count

IO & $08:202 & W – Port C Count

15 10	9 0
x	Transfer Count

IO & $08:203 & W – Port D Count

15 10	9 0
x	Transfer Count

IO & $08:204 & R/W – Skip Register

15 10	9	8	7	6-4	3	2	1	0
x	/RDYC	/RDYB	/RDYA	x	Skip D	Skip C	Skip B	Skip A

1=skip, 0=run

IO & $08:205 & R/W – EODC Register

15 4	3	2	1	0
x	EODC D	EODC C	EODC B	EODC A

1=repeat, 0=one-shot

IO & $08:206 & R – Status Register

15 4	3	2	1	0
x	D Bsy	C Bsy	B Bsy	A Bsy

IO & $08:207 & W – Reset DMAC

15 0
x

RXCHIP I/O

IO & $08:240 & R – Received Address Register

15 0
A15-A0

IO & $08:0241 & R – Received Data Register*

15 0
D15-D0

*Reading also clears the receiver interrupt

IO & $08:0242 & R – Hot-Link Status Register

15	14 6	5	4	3	2	1	0
Tick Sel	x	/DFF	/DEF	TCLK Carrier Det	/Slow	RX* Ovrn	TX** Loop

*Once set, RXOVRN requires a link-reset to clear
** TXLOOP is a divide-by-two of the Hot-Link tx test output

IO & $08:0243 & R – RX Test Loop Counter*

15 12	11 0
x	Count

*Requires a link-reset to clear

IO & $08:0244 & R – Received Error Counter*

15 12	11 0
x	Count

*Requires a link-reset to clear

IO & $08:0245 – DMAC Frame Tick Source Select

15	14 0
TICKSEL	x

IO & $08:0246 & R – 1 Mhz Free-running Counter, Low

15 0
FRC15-0

IO & $08:0247 & R – 1 Mhz Free-running Counter, High

15 0
FRC31-16

The FRC is latched by either a TCLK event (via the TCLK Correlation Event Register) or by a dummy write to the FRCH.

IP177 TCLK I/O

DM & $01:0000-00FF & W TeV Event Enable RAM

15 8	7	6	5	4	3	2	1	0
x	Enable on Ch7	Enable on Ch6	Enable on Ch5	Enable on Ch4	Enable on Ch3	Enable on Ch2	Enable on Ch1	Enable on Ch0

Low 8 bits of address is the event number

DM & $01:0100-0107 & W Timer 0-7 Control

15 8	7	6 5	4	3	2	1	0
x	Enable Trig	Timer Clock Select	GCTL 8*	Ena Boostr Reset Trig	Ext/Int Trig	Sync	Enable Chain Trig

*Global control bit 8 appears in TCTL1 only but affects all timers.
GCTL8: External/Internal Prescaler Reset

DM & $01:0108-010F & W Timer 0-7 Delay

15 0
Delay15-0

NOTE: Delay=0 disables the counter

DM & $01:0110-0117 & W Timer 0-7 Width

15	0
Width15-0	

NOTE: Width=0 disables the counter

DM & $01:0118-011F & W Timer 0-7 Software Trigger

15	0
x	

DM & $01:0130 & W Burst DMA Frame Count

15	0
Frames per Trigger Event, 0-65535	

A value of zero results in a single frame per trigger.

DM & $01:0138-013A & W Arm Port A-C

15	0
x	

DM & $01:013B & W TCLK Trigger Event

15	8	7	0
x		Trigger Event7-0	

DM & $01:013C & W TCLK DMA Event

15	8	7	0
x		DMA Event7-0	

DM & $01:013D & W TCLK Correlation Event

15	8	7	0
x		Correlation Event7-0	

DM & $01:013E & W Prescale Sync Event

15	8	7	0
x		Prescale Event7-0	

DM & $01:013F & W Global Control

15 8	7	6	5	4	3	2	1	0
x	TCLK Out Enable	10Mhz Out Enable	1Mhz Out Enable	Prescale Sync Ena	P.Sync Evt / BReset	Ext 10Mhz/ Int 10Mhz	Ext 10Mhz Enable	Gate Output Enable

GCTL0: Enables all gate outputs when 1
GCTL1: Selects ext. 10Mhz connector when 1, output of GCTL2 when 0
GCTL2: Selects int. 10Mhz source when 1, TCLK carrier when 0
GCTL5: Turns on 1Mhz at backpanel lemo
GCTL6: Turns on 10Mhz from GCTL1 at backpanel lemo
GCTL7: Repeats TCLK input to backpanel lemo

Virtual Register Assignments

PMC Adrs	Rcvd Adrs	Name	*R/W, size*	Maps to
48 0000	0000	Port A Module ID	R, w	DMC0 :0000
48 0002	0001	Port A Module Base Offset (from 48 0000)	R, w	Synthesized
48 0004	0002	Port A Correlation Event Time High	R, w	Synthesized
48 0006	0003	Port A Correlation Event Time Low	R, w	Synthesized
48 0008	0004	Port B module ID	R, w	DMC1:0000
48 000A	0005	Port B Module Base Offset (from 48 0000)	R, w	Synthesized
48 000C	0006	Port B Correlation Event Time High	R, w	Synthesized
48 000E	0007	Port B Correlation Event Time Low	R, w	Synthesized
48 0010	0008	Port C Module ID	R, w	DMC2 :0000
48 0012	0009	Port C Module Base Offset (from 48 0000)	R, w	Synthesized
48 0014	000A	Port C Correlation Event Time High	R, w	Synthesized
48 0016	000B	Port C Correlation Event Time Low	R, w	Synthesized
48 0018	000C			
48 001A	000D	RU Correlation Event Time High	R, w	Synthesized
48 001C	000E	RU Correlation Event Time Low	R, w	Synthesized
48 001E	000F			
48 0020	0010	RU Reset	W, w	Synthesized
48 0022	0011	Rx Test Loop Count	R, w	IO08:0243
48 0024	0012	Rx Error Count	R, w	IO08:0244
48 0040	0020	RU Link and TCLK Status	R, w	IO08:0242
48 0042	0021	RU Reset Status	R, w	Synthesized
48 0044	0022	RU Heartbeat Counter	R, w	Synthesized
48 0046	0024	Loop-thru back	R, w	Synthesized

48 0048	0026	Loop-thru out	W, w	Synthesized
48 0080	0040	DMA Frame Rate	RW,w	Synthesized
48 0082	0041	DMA Frame TCLK Trigger Enable	RW,w	Synthesized
48 0084	0042	RU Status Update Rate	RW,w	Synthesized
48 0086	0043	Digital Inputs Update Rate	RW,w	Synthesized
48 0088	0044	Firmware Version	R,w	Synthesized
48 0090	0048	IP177 Timer 0 Delay	RW,w	DM01:0108
48 0092	0049	IP177 Timer 0 Width	RW,w	DM01:0110
48 0094	004A	IP177 Timer 0 Control	RW,w	DM01:0100
48 0096	004B	IP177 Timer 0 Trigger	RW,w	DM01:0118
48 0098	004C	IP177 Timer 1 Delay	RW,w	DM01:0109
48 009A	004D	IP177 Timer 1 Width	RW,w	DM01:0111
48 009C	004E	IP177 Timer 1 Control	RW,w	DM01:0101
48 009E	004F	IP177 Timer 1 Trigger	RW,w	DM01:0119
48 00A0	0050	IP177 Timer 2 Delay	RW,w	DM01:010A
48 00A2	0051	IP177 Timer 2 Width	RW,w	DM01:0112
48 00A4	0052	IP177 Timer 2 Control	RW,w	DM01:0102
48 00A6	0053	IP177 Timer 2 Trigger	RW,w	DM01:011A
48 00A8	0054	IP177 Timer 3 Delay	RW,w	DM01:010B
48 00AA	0055	IP177 Timer 3 Width	RW,w	DM01:0113
48 00AC	0056	IP177 Timer 3 Control	RW,w	DM01:0103
48 00AE	0057	IP177 Timer 3 Trigger	RW,w	DM01:011B
48 00B0	0058	IP177 Timer 4 Delay	RW,w	DM01:010C
48 00B2	0059	IP177 Timer 4 Width	RW,w	DM01:0114
48 00B4	005A	IP177 Timer 4 Control	RW,w	DM01:0104
48 00B6	005B	IP177 Timer 4 Trigger	RW,w	DM01:011C
48 00B8	005C	IP177 Timer 5 Delay	RW,w	DM01:010D
48 00BA	005D	IP177 Timer 5 Width	RW,w	DM01:0115
48 00BC	005E	IP177 Timer 5 Control	RW,w	DM01:0105
48 00BE	005F	IP177 Timer 5 Trigger	RW,w	DM01:011D
48 00C0	0060	IP177 Timer 6 Delay	RW,w	DM01:010E
48 00C2	0061	IP177 Timer 6 Width	RW,w	DM01:0116
48 00C4	0062	IP177 Timer 6 Control	RW,w	DM01:0106
48 00C6	0063	IP177 Timer 6 Trigger	RW,w	DM01:011E
48 00C8	0064	IP177 Timer 7 Delay	RW,w	DM01:010F
48 00CA	0065	IP177 Timer 7 Width	RW,w	DM01:0117
48 00CC	0066	IP177 Timer 7 Control	RW,w	DM01:0107
48 00CE	0067	IP177 Timer 7 Trigger	RW,w	DM01:011F
48 00D0	0068	IP177 Prescale Sync Event	RW,w	DM01:013E
48 00D2	0069	IP177 Global Control	RW	DM01:013F
48 00D4	006A	Arm Port A	RW	DM01:0138
48 00D6	006B	Arm Port B	RW	DM01:0139
48 00D8	006C	Arm Port C	RW	DM01:013A
48 00DA	006D	TCLK Correlation Event	RW,w	DM01:013D

48 00DC	006E	TCLK Trigger Event	RW,w	DM01:013B
48 00DE	006F	TCLK DMA Event	RW,w	DM01:013C
48 00E0	0070	Burst DMA Frame Count	RW,w	DM01:0130
48 0200-02FF	0100-01FF	TCLK Event Enable RAM*	RW, w,b	DM01:0000-00FF

*Each byte in PMC space maps to a single 16 bit word in the event RAM

Remote Unit Reset Register, $48 0020

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
rst link	x	x	x	x	x	rst ack	wdt rst	x	x	x	x	x	x	x	soft rst

Writes to this register that have multiple bits set are ignored.
"soft rst" initates a software reboot through the DSP SWRST register.
"wdt rst" puts the DSP into an endless loop until the watchdog timer does a hardware reset.
"rst ack" clears the reset status at 0x48 0042.
"rst link" resets the serial link only.

Remote Unit Reset Status Register, $48 0042

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
177 crc	C crc	B crc	A crc	ctl crc	plink crc	x	rst	x	x	x	x	x	x	x	soft rst

"soft rst" is set when the reboot is the result of a "soft rst" command via 0x48 0020.
"rst" is set after any reboot.
CRC flags are set during reboot to indicate that the corresponding blocks of BBSRAM passed a CRC check.

Remote Unit Link and TCLK Status Register, $48 0040

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	x	x	x	x	x	x	x	x	TCK CD	/slow	rx ovrn	tx loop

DMA Frame Rate Register, $48 0080

DMA frame timer period in microseconds. Default is 100 microseconds. Values less than 100usec are ignored.

DMA Frame Trigger Source Register, $48 0082

When non-zero, DMA is initiated by the DMA TCLK Event ($48 00DE). When zero, DMA is initiated by the internal timer.

Remote Unit Status Update Rate, $48 0084

Determines the number of DMA frames between each update of the RU status registers ($48 0040-0049). For example, a value of 2 will update the status every other frame, 3 every third frame,etc. Default is 1 (every frame).

Port D Update Rate, $48 0086
Determines the number of DMA frames between each update of the IOM control and status registers. For example, a value of 2 will update the status every other frame, 3 every third frame,etc. Default is 1 (every frame).

X. 64-bit Digital IO Module ("Digio")

The Digital I/O module interfaces 64 bits of digital I/O through the use of 8, 8 bit wide R/W data registers. Each register is individually addressable and can be configured as input or output port by writing to an internal 8 bit data direction register.

Two bytes of digital data are connected each of four 37-pin D type connectors accessible from the back panel. Data transfer is into the module is word wide. I/O data transfer is byte wide. In addition to the I/O ports, two Form C relays are accessible through two, 3-pin Molex headers, also on the back panel. With the exception of the relays, all I/O is non-isolated. Each output can sink up to 64mA and source up to 32mA. Inputs are TTL compatible with input current of +/-20uA.

Three actions will clear all registers and set the I/O ports to all input: 1) A reset generated from power up, 2) Resetting the HRMII, 3) Local onboard reset via a tact switch.

Board Address Space
Base + 0x00, Read-only
Module ID Register

15 8	7 0
Module ID = 0x4E	Module Revision Number = 0x01

Base + 0x01, Read/Write
Test Register

15 8	7 0
x	Test

Base + 0x02, Read/Write, Relay 0 Register
Base + 0x03, Read/Write, Relay 1 Register

15 1	0
x	Relay On

Base + 0x04, Read/Write
Data Direction Register

15 8	7	6	5	4	3	2	1	0
x	Port 7	Port 6	Port 5	Port 4	Port 3	Port 2	Port 1	Port 0

0=all bits input, 1=all bits output

Base + 0x05 through Base + 0x17 Not Used

Base + 0x18 through 0x1F, Read/Write
Ports 0 through 7

15 8	7	6	5	4	3	2	1	0
x	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0

VME Address Space at PMC

Base plus module offset plus	Register
0x0, 0x1	Module ID
0x2, 0x3	Test
0x4, 0x5	Relay 1
0x6, 0x7	Relay 2
0x8, 0x9	Data Direction Register
0xA-0x37	x
0x38	Data Register 0
0x39	Data Register 1
0x3A	Data Register 2
0x3B	Data Register 3
0x3C	Data Register 4
0x3D	Data Register 5
0x3E	Data Register 6
0x3F	Data Register 7

Address to Connector Mapping

Port Address	Controlled by DDR (0x04) Bit	IO Connector (LSB---MSB)	Strobe Output	Direction Output
0x18	0	P4-1 through 8	P4-19	P4-37
0x19	1	P4-9 through 16	P4-18	P4-37
0x1A	2	P3-1 through 8	P3-19	P3-37
0x1B	3	P3-9 through 16	P3-18	P3-37
0x1C	4	P2-1 through 8	P2-19	P2-37
0x1D	5	P2-9 through 16	P2-18	P2-37
0x1E	6	P1-1 through 8	P1-19	P1-37
0x1F	7	P1-9 through 16	P1-18	P1-37

I/O Signals

STB07-STB00	Output	100ns positive pulse. Output data is valid on falling edge.
DIR03-DIR00	Output	Data direction for the port accessed. Active on the falling edge of STB
B8-B0	Bi-directional	Bit 8 – 0

Register Descriptions and Operation

Board ID

A 16 bit read-only register resides in a FLEX 10K20 FPGA. It is set to 0x4E01.

Data Direction Register (DDR)

Ports are programmable by writing to the DDR. Writing the register stores the low 8 bits of a 16-bit word. The LS bit represents I/O port 0. Setting a bit programs the associated port as an output. All bits are cleared to 0 (input) upon reset. A series of LED's are onboard to reflect the current state of each port. Green indicates the port is programmed as input, red indicates an output port. These LED's are a diagnostic aid and are not viewable from outside the cabinet.

Data Registers

Data is stored by writing to a 16 bit bi-directional transceiver configured as two eight bit transceivers. Onboard D type flip-flops make up each data register. The result of writing to a data register depends on the configuration of the port associated with the register. If the port is configured as an output, data is stored and the output drivers enabled. If the port is configured as an input no action is taken. Reading a data register that is configured as an output always reads the state of the connector pin and not the state of the output latch.

Relay Registers

Each register is a single bit in D0. Setting the bit will activate the relay, clearing it will deactivate it. The bit must remain set to hold the relay energized.

Test

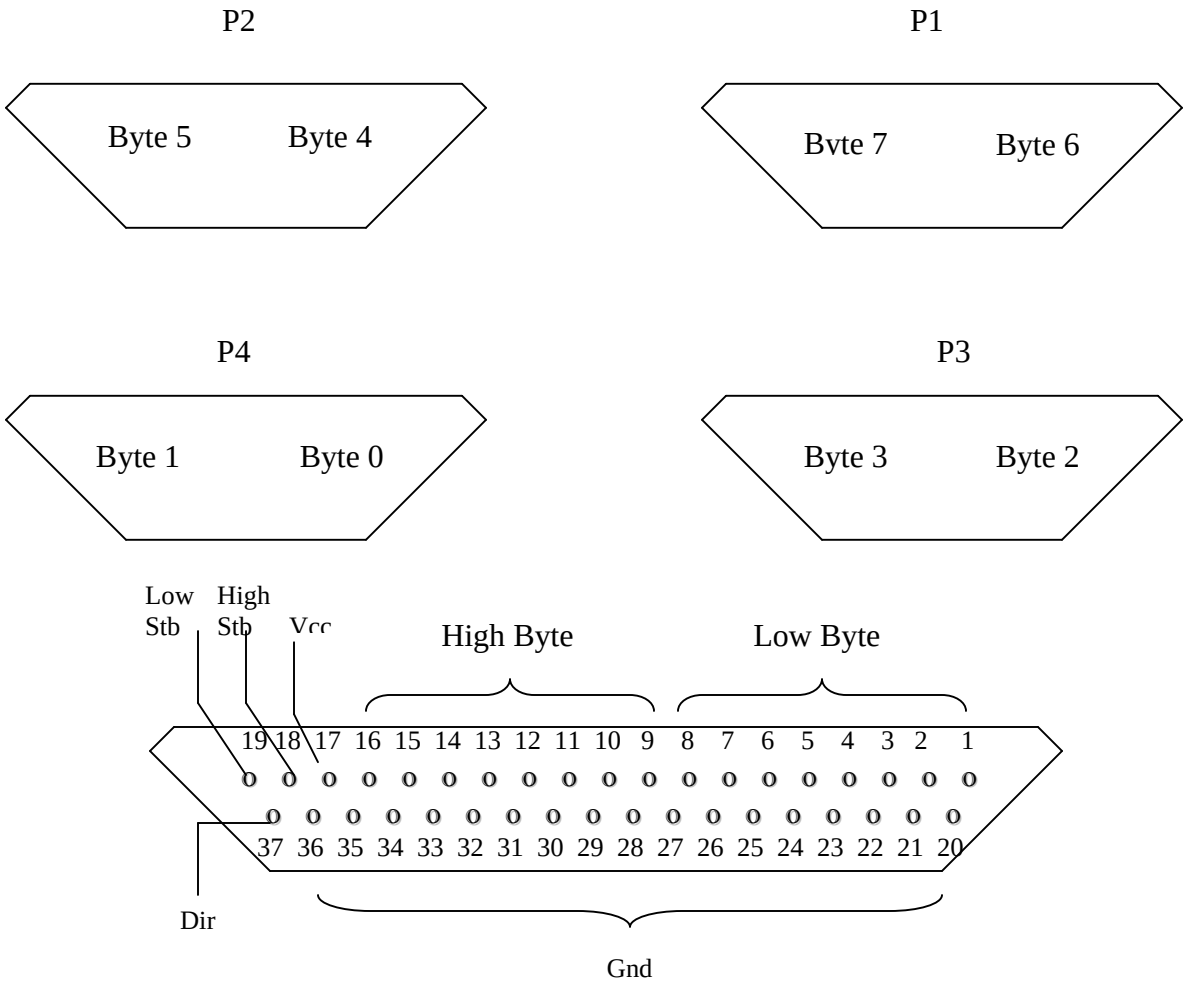
The test register is an 8 bit read/write port.

Form C Relays

Each relay has a maximum rating of 1 amp at 110v. The operating function of each relay is single side stable. Writing a 1 to a relay register will turn on the relay. The relays are not of the latching type; therefore the relay coil must remain energized for the relay to operate. Writing a 0 to a register will deenergize the relay.

Connector Pinouts

Each 37 pin D connector is associated with 2 bytes of I/O. There are 3 additional output signals. There are two strobes for each of the two bytes and one direction signal for both bytes. If direction = 0 the port being accessed is an output. Only 1 byte is accessible at a time so strobe and direction signals must be used together to select the proper byte.



XI. MADC-64 64 Channel 10Khz Multiplexed Analog-to-Digital Converter

The MADC-64 card accepts 64 channels of analog inputs for digitization at rates of up to 160 Khz and provides 8 channels of analog output.

Byte-writes cannot be used when writing an MADC-64 through the HRM PMC; all writes must be word (16 bit) or long (32 bit).

Timestamp

A free-running 32-bit counter is clocked at 1 Mhz to provide a timestamp of 1 usec resolution. Timestamp data is acquired and travels with its corresponding channel samples. The timestamp is correlated to a TCLK event by the DSP on the HRM central board.

ADC Operation

Input channels are grouped in sets of 16 and presented to four DG506 multiplexers. The output of each mux drives an AD976 16-bit analog-to-digital converter. Sixty-four measurements are taken by the ADCs during each acquisition cycle of typically 100 usec. By manipulating the mux controls, these measurements can be distributed over all 64 inputs or over subsets of fewer channels to increase the sampling rate of a smaller number of inputs. Because acquisition is synchronous with the HRM DMA rate, slower sampling rates can be achieved by slowing the HRM DMA rate. A test mode feeds derived from the timestamp counter into the ADC datapath to verify the integrity of the entire HRM system, from the MADC card to the VME chassis. The ADCs are not accessible to the HRM DSP; ADC data streams directly to the HRM DMA channel.

DAC Operation

Two four-channel 16-bit digital-to-analog converters are mapped into DSP off-chip DM space. Their outputs are bipolar with 0x0 producing –5.000v and 0xFFFF producing +5.000v.

(The HRM DSP applies an offset so that the DACs appear to be 2s-complement at the PMC)

Scan Control Register Settings

Value	Mode	Active Channels	Sample Rate at 10Khz DMA rate
0	64 channel	All	10 Khz
1	32 channel	0-7, 16-23, 32-39, 48-55	20 Khz
2	16 channel	0-3, 16-19, 32-35, 48-51	40 Khz
3	8 channel	0-1, 16-17, 32-33, 48-49	80 Khz
4	4 channel	0, 16, 32, 48	160 Khz

5	Test 0	Timestamp-derived data	NA
6	Test 1	Ramp	NA

Test mode 0 data formatting:

During test mode 0, the low 14 bits of the timestamp counter are inverted and routed into the data paths of the four ADCs. The ADCs fire rapidly in succession but then wait 6.25 usec until the next acquisition. ADC data will decrease 6 or 7 counts from channel to channel within a "quadrant" (channels 0-15, 16-31, 32-47, 48-63). Channels in different quadrant but having the same offset will have equal values. To guarantee that each channel has unique data, the top two bits (15:14) reflect their respective quadrant:

Channel	D[15:14]
0-15	00
16-31	01
32-47	10
48-63	11

D[13:08] = ~(TIMESTAMP[21:16])
D[07:00] = ~(TIMESTAMP[07:00])

Test mode 1 data formatting:

Data comes from a counter that increments with each ADC conversion. When data reaches 0xFFFF, the value wraps to 0x0040.

Channel_N_ data = Channel_(N-1)_ data +1

HRM Central Board Address Space

Base + 0x00 & Read
Module ID Register

15 8	7 0
Module ID = 0x72	Module Revision Number = 0x01

Base + 0x00 & Write
Module Typecodes Register

15 8	7 4	3 0
x	Timestamp TC	Data TC

Base + 0x01, Read/Write
Scan Control Register

15 3	2 0
x	Scan Ctrl

0 = 64ch (0-63)
1 = 32ch (0-7, 16-23, 32-39, 48-55)
2 = 16ch (0-3, 16-19, 32-35, 48-51)
3 = 8ch (0-1, 16-17, 32-33, 48-49)
4 = 4ch (0, 16, 32, 48)
5 = test

Base + 0x02, Read Only, Timestamp Low

15 0
Timestamp

Reading this register also latches the high word of the timestamp

Base + 0x03, Read Only, Timestamp High

15 0
Timestamp

Base + 0x04, Read Only, FPGA version

15 0
FPGA version

Base + 0x08 through 0x0F, Write Only
DAC0-7

15 0
DAC Data

0x0 = -5.000V, 0xFFFF = +5.000V

VME Address Space at PMC *(int and long int only)*

Base plus module offset	Register
0x0, 0x1	Module ID
0x2, 0x3	Scan Control
0x4, 0x5	x
0x6, 0x7	x
0x8, 0x9	x
0xA, 0xB	Remote-unit-assigned data typecode
0xC, 0xD	Remote-unit-assigned timestamp typecode
0xE,0xF	x
0x10, 0x11	DAC0
0x12, 0x13	DAC1

0x14, 0x15	DAC2
0x16, 0x17	DAC3
0x18, 0x19	DAC4
0x1A, 0x1B	DAC5
0x1C, 0x1D	DAC6
0x1E, 0x1F	DAC7

Note:
DACs are restored at reset to the last written value. Uninitialized/reinitialized DACS are set to 0x8000 = 0.000v

DAC Connector Pinout

(A is the upper connector, B is the lower connector)

Pin Nr	P4A	P4B
1	DAC4	DAC0
2	DAC5	DAC1
3	DAC6	DAC2
4	DAC7	DAC3
5-9	AGND	AGND

ADC Connector Pinout

(A is the upper connector, B is the lower connector)

Pin Nr	P5A	P5B	P6A	P6B
1	Ch 32+	Ch 0+	Ch 48+	Ch 16+
2	Ch 33+	Ch 1+	Ch 49+	Ch 17+
3	Ch 34+	Ch 2+	Ch 50+	Ch 18+
4	Ch 35+	Ch 3+	Ch 51+	Ch 19+
5	Ch 36+	Ch 4+	Ch 52+	Ch 20+
6	Ch 37+	Ch 5+	Ch 53+	Ch 21+
7	Ch 38+	Ch 6+	Ch 54+	Ch 22+
8	Ch 39+	Ch 7+	Ch 55+	Ch 23+
9	Ch 40+	Ch 8+	Ch 56+	Ch 24+
10	Ch 41+	Ch 9+	Ch 57+	Ch 25+
11	Ch 42+	Ch 10+	Ch 58+	Ch 26+
12	Ch 43+	Ch 11+	Ch 59+	Ch 27+
13	Ch 44+	Ch 12+	Ch 60+	Ch 28+
14	Ch 45+	Ch 13+	Ch 61+	Ch 29+
15	Ch 46+	Ch 14+	Ch 62+	Ch 30+
16	Ch 47+	Ch 15+	Ch 63+	Ch 31+
17	(nc)	(nc)	(nc)	(nc)
18	(nc)	(nc)	(nc)	(nc)
19	(nc)	(nc)	(nc)	(nc)
20	Ch 32-	Ch 0-	Ch 48-	Ch 16-

21	Ch 33-	Ch 1-	Ch 49-	Ch 17-
22	Ch 34-	Ch 2-	Ch 50-	Ch 18-
23	Ch 35-	Ch 3-	Ch 51-	Ch 19-
24	Ch 36-	Ch 4-	Ch 52-	Ch 20-
25	Ch 37-	Ch 5-	Ch 53-	Ch 21-
26	Ch 38-	Ch 6-	Ch 54-	Ch 22-
27	Ch 39-	Ch 7-	Ch 55-	Ch 23-
28	Ch 40-	Ch 8-	Ch 56-	Ch 24-
29	Ch 41-	Ch 9-	Ch 57-	Ch 25-
30	Ch 42-	Ch 10-	Ch 58-	Ch 26-
31	Ch 43-	Ch 11-	Ch 59-	Ch 27-
32	Ch 44-	Ch 12-	Ch 60-	Ch 28-
33	Ch 45-	Ch 13-	Ch 61-	Ch 29-
34	Ch 46-	Ch 14-	Ch 62-	Ch 30-
35	Ch 47-	Ch 15-	Ch 63-	Ch 31-
36	AGND	AGND	AGND	AGND
37	AGND	AGND	AGND	AGND

XII. 10MHz, 8 Channel Snapshot Digitizer

HRM Central Board Address Space

Base + 0x00 & Read
Module ID Register

15 8	7 0
Module ID = 0x1D	Module Revision Number = 0x00

Base + 0x00 & Write
Module Typecodes Register

15 8	7 4	3 0
x	Timestamp TC	Data TC

Base + 0x01, Read/Write
Channel Scan

15 2	1 0
x	Cnl Scan

0 = Normal operation
1 = Ramp mode: ADC Data[15:13] Channel Nr, ADC Data[12:00] Ramp
2 = Channel Number Stamp: Cnl 0 Data=0x0FF0, Cnl 1=0x1FF1, …
3 = (reserved)

Base + 0x02, Read Only, Timestamp Low

15	0
Timestamp	

Reading this register also latches the high word of the timestamp

Base + 0x03, Read Only, Timestamp High

15	0
Timestamp	

Base + 0x04, Read Only, FPGA version

15	0
FPGA version	

Base + 0x05, Read/Write, ADC Control

15	0

15:11 – (reserved)
10:08 – ADC Sample Rate
00x = 10MHz or Ext Clock
010 = 5MHz or Ext Clock/2
011 = 2.5MHz or Ext Clock/4
100 = 1.25MHz or Ext Clock/8
101 = 625KHz or Ext Clock/16
110 = 312KHz or Ext Clock/32
111 = 156KHz or Ext Clock/64
07:05 – (reserved)
04 - Auto Trigger, 0=Single Shot(A,T,A,T,…), 1=Auto Trigger(A,T,T,T,…)
03:02 – ADC Sample and Delay Timer Clock Source
00 = Internal Oscillator
01 = TCLK Carrier (fails over to internal oscillator if TCLK is lost)
1x = External Clock
01:02 – ADC Acquisition Trigger Source
00 = Event + Delay
01 = External Trigger
10 = TCLK Pre-trigger/Trigger Event Sequence
11 = Software Trigger

Base + 0x06, Read/Write, ADC Sample Count

15	14	0
x	Sample Count (0x1 - 0x4000)	

Base + 0x07, Read/Write, Delay Timer Control

15 4	3 2	1 0
x	Timer Pre-Divide	Delay Start Source

Timer Pre-Divide

00 = 1
01 = 10
10 = 100
11 = 1000

Delay Start Source

x0 = Booster Reset Event
01 = Programmable TCLK Event
11 = External Trigger

Base + 0x08, Read/Write, Delay Timer Duration

15 0
Delay Duration, counts

Base + 0x09, Read/Write, TCLK Pre-Trigger Event

15 8	7 0
x	TCLK Event

Base + 0x0A, Read/Write, TCLK Trigger Event

15 8	7 0
x	TCLK Event

Base + 0x0B, Read/Write, TCLK Trigger Event Count Preset

15 8	7 0
x	Count Preset

Base + 0x0E, Write Only, Manual Arm

15 0
x

Base + 0x0F, Write Only, Trigger Parameter Capture

15 0
x

Any write to this register causes the trigger generator and TCLK deserializer to capture trigger parameters previously written to addresses 0x05 through 0x0B. The acquisition in progress is terminated and the trigger generator will wait for an ARM.

Base + 0x10, Read Only, Acquisition Status

15 6	5 0
x	Status

Status[0]: Armed
Status[1]: Trigger received, acquisition in progress
Status[2]: Acquisition complete
Status[3]: FIFO empty
Status[4]: TCLK sequence pre-trigger received
Status[5]: TCLK carrier present

Base + 0x11, Read Only, FIFO Write Count

15 0
FIFO Write Count

Base + 0x12, Read Only, FIFO Read Count

15 0
FIFO Read Count

Base + 0x13, Read Only, Trigger Delay Count

15 0
Trigger Delay Count

Base + 0x14, Read Only, TCLK Trigger Event Count

15 0
TCLK Trigger Event Count

VME Address Space at PMC *(int only)*

Base plus module offset	Attrib.	Register
0x0, 0x1	R,w	Module ID
0x2, 0x3	RW,w	Channel Scan
0x4, 0x5	R,w	Timestamp low
0x6, 0x7	R,w	Timestamp high
0x8, 0x9	R,w	FPGA version
0xA, 0xB	RW,w	ADC Control
0xC, 0xD	RW,w	ADC Sample Count
0xE, 0xF	RW,w	Delay Timer Control
0x10, 0x11	RW,w	Delay Timer Duration
0x12, 0x13	RW,w	TCLK Pre-trigger Event
0x14, 0x15	RW,w	TCLK Trigger Event
0x16, 0x17	RW,w	TCLK Trigger Event Preset
0x18, 0x19	x	(not used)

0x1A, 0x1B	x	(not used)
0x1C, 0x1D	W,w	Manual Arm
0x1E, 0x1F	W,w	Trigger Parameter Capture
0x20, 0x21	R,w	Acquisition Status
0x22, 0x23	R,w	FIFO Write Count
0x24, 0x25	R,w	FIFO Read Count
0x26, 0x27	R,w	Trigger Delay Count
0x28, 0x29	R,w	TCLK Trigger Event Count

XIII. Boot Options and HRM Monitor

After a hardware reset the HRM prompts the user through the serial port to enter "B" for continue booting, "C" for clear all battery-backed SRAM, and "P" to re-program the EEPROM. After waiting about 10 seconds the HRM will continue to boot.

The HRM run-time monitor gives direct access to the SRAM and IO spaces for debug:

```
DR pp aaaa              DM          read     page, address
DW pp aaaa nnnn         DM          write    page, address, 16-bit data
DD pp aaaa bbbb         DM          read     multiple page from aaaa to
bbbb
DF pp aaaa bbbb nnnn    DM          write    fill page from aaaa to bbbb
with 16-bit data
IR pp aaaa              IO          read     page, address
IW pp aaaa nnnn         IO          write    page, address, 16-bit data
HE                      Help listing
+                       Increment aaaa or nn and repeat the last command
-                       Decrement aaaa or nn and repeat the last command
=                       Repeat the last command
```

XIV. ROM Monitor

A ROM monitor is available that boots from the EEPROM, "MON2191". The monitor provides some basic commands to manipulate program memory, data memory, I/O, and processor core registers. A download facility accepts files in standard Analog Devices UART bootloader format. A CALL and a GO command allow a user to test code directly on a HRM target without an in-circuit emulator.

While functions within the monitor do not conform with the ADI C conventions, the monitor does not use any of the C dedicated or preserved registers.

A Note About the ADSP2191 Bootloader

Both the on-chip bootloader and MON2191 implement off-chip fills (flag=0011) and initializations (flag=0015). However, the on-chip loader thinks that the external bus is byte-wide so it doubles the load address and the segment length, placing fills and data in the wrong place. MON2191 knows that the external bus is word-wide and correctly places the data.

Systems will ultimately rely on the on-chip bootloader. Thus, any off-chip tables must be explicitly set up by code and zero-fill of off-chip DM must be done from a program loop.

The Python utility, loader.py, used to combine multiple hex files into a single boot file, suppresses all boot records with the 11 or 15 flags.

Monitor Location

After boot, the monitor occupies 0x7B00-0x7F15 in on-chip program memory and 0xFEE0-0xFEEC in on-chip data memory (0xFF00-0xFFFF are reserved by the ADI bootloader ROM).

Useful Entry Addresses

get_byte_ax1	0x7b41
get_char_ax1	0x7b16
get_le_word_ax1	0x7b8a
get_next_ax1	0x7b60
get_nibble_ax1	0x7b28
get_word_ax1	0x7b4b
out_byte_ax1	0x7ba2
out_char_ax1	0x7b0d
out_nibble_ax1	0x7b98
out_word_ax1	0x7bad
sendLine	0x7bc5

These routines generally step on the accumulator registers and the shifter registers. See code listings for details.

Monitor Commands
(lower case=user entries, upper case=monitor response; monitor input is case-insensitive)

C: Call user program

Call a subroutine using a user-entered memory page and address

*cppaaaa!
- pp – memory page
- aaaa – subroutine address
- ! – monitor acknowledgement

D: DM display and modify

Display and modify data memory

*dppaaaa NNNN [<sp> | . | , | mmmm][<sp> | . | ,]

pp – memory page pointer
aaaa – initial memory address pointer
NNNN – current location content
<sp> - advances pointer to the next sequential address
, - moves pointer to previous address
. – leaves pointer at current address
mmmm – new memory value

Address rollover from 0xFFFF to 0x0000 or from 0x0000 to 0xFFFF does not change the page pointer

G: Run user program

Execute a user program by jumping through the restart vector at PM0x000000

*g!
! – monitor acknowledgement

H: Help listing

Print a list of monitor commands

*h
C: CALL USER PROGRAM
D: DM DISPLAY AND MODIFY
G: RUN USER PROGRAM
H: HELP LISTING
I: READ INPUT PORT
L: LOAD UART BOOTSTREAM
M: DM DUMP
O: WRITE OUTPUT PORT
P: PM DISPLAY AND MODIFY
R: EDIT CORE REGISTERS

I: Read input port

Read and print the value of a port in I/O space

*ipp aaaa NNNN[.]

pp – I/O page pointer
aaaa – I/O port address
NNNN – current value of the port
. – read and display the port value again

L: Load UART bootstream

Load a standard Analog bootstream file into memory via the serial port (see Analog Devices Engineer-to-Engineer Note EE-131, “Booting the ADSP-2191” for a description of the boot file format. Note that MON2191 does not autobaud and will become confused if it sees an added 0xAA character at the beginning of the download.

*l!

! – monitor acknowledgment

M: DM dump

List up to 1024 words of data memory

*mppaaaa
PPAAAA NNNN
.
.
.
PPAAAA NNNN

pp – memory page pointer
aaaa – initial memory address pointer

Address rollover from 0xFFFF to 0x0000 or from 0x0000 to 0xFFFF does not change the page pointer

O: Write output port

Write a value to a port in I/O space

*opp aaaa nnnn[.]

pp – I/O page pointer
aaaa – I/O port address
nnnn – new value of the port
. – write the port value again

P: PM display and modify

Display and modify program memory

*pppaaaa NNNNNN [<sp> | . | , | mmmmmm] [<sp> | . | ,]

pp – memory page pointer
aaaa – initial memory address pointer

NNNNNN – current location content
<sp> - advances pointer to the next sequential address
, - moves pointer to previous address
. – leaves pointer at current address
mmmmmm – new memory value

Address rollover from 0xFFFF to 0x0000 or from 0x0000 to 0xFFFF does not change the page pointer

R: Edit core registers

Read and modify the contents of the DSP core registers

*r
RGP:a REG ADRS:b NNNN mmmm

a – register group, 0-3, per table
b – register address, 0-F, per table
NNNN – current register value
mmmm – new register value

Note that because this command modifies core registers, strange and unusual things may happen when register values are changed. Because the monitor uses the accumulator, the shifter, and DAG2, reading these registers may yield meaningless numbers and writing to these registers may be futile.

RGP/Address	Register Groups			
Address	0 (DREG)	1 (REG)	2 (REG2)	3 (REG3)
0	AX0	I0	I4	ASTAT
1	AX1	I1	I5	MSTAT
2	MX0	I2	I6	SSTAT
3	MX1	I3	I7	LPSTACKP
4	AY0	M0	M4	CCODE
5	AY1	M1	M5	SE
6	MY0	M2	M6	SB
7	MY1	M3	M7	PX
8	MR2	L0	L4	DMPG1
9	SR2	L1	L5	DMPG2
A	AR	L2	L6	IOPG
B	SI	L3	L7	IJPG
C	MR1	IMASK	Reserved	Reserved
D	SR1	IRPTL	Reserved	Reserved
E	MR0	ICNTL	CNTR	Reserved
F	SR0	STACKA	LPCSTACKA	STACKP